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AF/2186

PATENT APPLICATION

ATTORNEY DOCKET NO. 10004121-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Jeffrey G. Hargis, et al.

Confirmation No.: 5760

Application No.: 09/828,041

Examiner: Kim, Hong Chong

Filing Date: 04-07-2001

Group Art Unit: 2186

Title: MEMORY CONTROLLER RECEIVER CIRCUITRY WITH TRI-STATE NOISE IMMUNITY

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **July 9, 2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Signature: _____

Respectfully submitted,

Jeffrey G. Hargis, et al.

By _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	09/828,041	Confirmation No. 5760
Appellant	:	Jeffrey G. Hargis, et al.	
Filed	:	April 7, 2001	
TC/A.U.	:	2186	
Examiner	:	Kim, Hong Chong	
Docket No.	:	10004121-1	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

APPEAL BRIEF

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	09/828,041	Confirmation No. 5760
Appellant	:	Jeffrey G. Hargis, et al.	
Filed	:	April 7, 2001	
TC/A.U.	:	2186	
Examiner	:	Kim, Hong Chong	
Docket No.	:	10004121-1	

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated March 15, 2004.

Appellants filed a Notice of Appeal on July 9, 2004.

Real Party in Interest

The real party in interest is Hewlett-Packard Company, assignee of the above-captioned patent application. Hewlett-Packard Company is a Delaware Corporation having its principal place of business in Palo Alto, California.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1-42 are pending. Of these, claims 12-28 and 33-42 have been allowed. Claims 7, 8, 10, 11, 31 and 32 stand objected to as being dependent on one or more rejected claims, but are otherwise allowable. Claims 1-6, 9, 29 and 30 stand rejected. A copy of Appellants' claims is attached as an Appendix to this Appeal Brief.

Appellants appeal from the Examiner's rejection of claims 1-6, 9, 29 and 30.

Status of Amendments

Claims 12, 16, 33 and 36 were amended in an Amendment dated December 19, 2003. This Amendment has been entered. There are no un-entered amendments.

Summary of Invention

The invention is variously embodied. In one embodiment, strobe receiver circuitry (p. 37, line 4 – p. 47, line 30; FIGS. 19 & 20) comprises a counter (1900, FIG. 19; 2000, 2002, FIG. 20) and counter control logic (1902, FIG. 19; 2004-2028, 2032-2038, FIG. 20). The counter updates a count in response to strobe edges of received strobe signals (DQS18). The counter control logic enables the counter before each strobe signal is received by generating control signals (DQS18_start, DQS18_ttf_rise_rst) asynchronously with respect to the received strobe signals (p. 38, lines 8-22). The counter control logic also resets the counter after each strobe signal is received by receiving feedback (1906, FIG. 19) from the counter and, in response to the feedback, resetting the counter asynchronously with respect to the received strobe signals (e.g., via stb_reset and DQS18_ttf_rise_rst, FIG. 20; p. 38, lines 23 – p. 39, line14; p. 42, line 22).

Issues

1. Whether claims 1-6 and 9 should be rejected under 35 U.S.C. 102(b) as being anticipated by CD4018B CMOS counter, TI Data Sheet, 1998.

2. Whether claims 1-6, 9, 29 and 30 should be rejected under 35 U.S.C. 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

Grouping of Claims

The rejected claims are grouped as follows:

Group I: Claims 1-6, 29 and 30

Group II: Claim 9

Argument

1. Whether claims 1-6 and 9 should be rejected under 35 U.S.C. 102(b) as being anticipated by CD4018B CMOS counter, TI Data Sheet, 1998 (hereinafter referred to as the "TI Data Sheet").

Appellants' claim 1 recites "counter control logic" that 1) *asynchronously* enables a counter "before *each* strobe signal is received", and 2) *asynchronously* resets the counter "after *each* strobe signal is received by receiving feedback from said counter". The Examiner asserts that such counter control logic is disclosed in the TI Data Sheet, wherein FIG. 15 shows the use of a PRESET input to enable a counter, and wherein FIG. 17 shows how to reset the counter using counter feedback. Appellants respectfully disagree.

To begin, Appellants note that their claim 1 is set in the context of "strobe receiver circuitry" that counts strobe edges of "each" of a number of received strobe signals. Although the counter described by the TI Data Sheet may be enabled and reset, the TI Data Sheet fails to describe any use of the CD4018B counter wherein the counter is enabled and reset in response to *each* of a number of strobe signals. Rather, each disclosed used of the CD4018B counter seems to presuppose that the counter's clock input will receive a *single, continuous clock signal (*see, e.g., the exemplary clock signal (CLOCK) shown in FIG. 15). In other words, although the CD4018B counter may certainly be enabled and reset, the TI Data Sheet does not disclose any use of the CD4018B counter wherein the counter is enabled and reset in relation to starts and stops of "each" of a number of strobe signals.

Appellants further note that the counter control logic of their claim 1 resets a counter "by receiving feedback from [the] counter and, in response to [the] feedback, resetting [the] counter *asynchronously* with respect to. . .received strobe signals". The Examiner asserts that FIG. 17 of the TI Data Sheet illustrates such a feedback system. Appellants respectfully disagree. The feedback system shown in FIG. 17 of the TI Data Sheet is a *synchronous* feedback system. That is, the only input to the feedback system is the clock CL. Appellants' claim 1, on the other hand, recites an asynchronous reset that is merely responsive to counter feedback. As disclosed in

Appellants' specification, such a reset is useful in that it enables counter control logic to count different numbers of received strobe edges, yet not count phantom strobe edges that are produced as a result of noise (see, e.g., Appellants' specification at p. 37, line 28 – p. 38, line 7; and p. 44, lines 5-12). With the counter disclosed in FIG. 17 of the TI Data Sheet, there is no way for the counter to count different numbers of strobe edges (even assuming, *arguendo*, that the TI Data Sheet anticipates the counter receiving each of a number of different strobe signals, which it does not).

Appellants also disagree with the Examiner's assertion that the counter disclosed in FIG. 17 of the TI Data Sheet is "reset", as that term is used by Appellants. Rather, the counter shown in FIG. 17 merely cycles through a number of states and periodically "rolls over". Appellants do not view this "roll over" functionality as being equivalent to a "reset". Appellants note that the reset (R) input of the FIG. 17 counter is tied to ground – which is presumably a conscious design choice to ensure that the counter *continues counting and does not reset.*

For the above reasons, Appellants' claim 1 is believed to be allowable over the teachings of the TI Data Sheet.

Appellants' claims 2-4 are believed to be allowable at least for the reason that they depend from claim 1.

Appellants' claim 5 is believed to be allowable over the teachings of the TI Data Sheet for reasons similar to those that make claim 1 allowable over the TI Data Sheet. That is, the TI Data Sheet does not teach nor suggest "counter control logic" that 1) *asynchronously* enables a counter "before *each* strobe signal is received", and 2) *asynchronously* resets the counter "after *each* strobe signal is received by i) receiving feedback from said counter".

Appellants' claims 6 and 9 are believed to be allowable over the teachings of the TI Data Sheet at least for the reason that they depend from claim 5. Claim 9 is also believed to be allowable in that the TI Data Sheet does not disclose "start and stop conditions [being] generated on a single signal line". Rather, the TI Data Sheet only discloses a counter with separate RESET and PRESET inputs, with no connection therebetween.

2. Whether claims 1-6, 9, 29 and 30 should be rejected under 35 U.S.C. 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

Appellants' claim 1 recites "counter control logic" that 1) enables a counter "before *each* strobe signal is received", and 2) resets the counter "after *each* strobe signal is received". The Examiner asserts that such counter control logic is described by Manning in col. 2, lines 39-51 (and, especially, in col. 2, lines 39-40). Appellants respectfully disagree.

Although the Examiner correctly notes that Manning discloses the enablement and disablement of a counter in response to a "start signal" and a "stop signal", Manning also states the following:

> . . .the Counter 50 is an 8 stage quadrature counter which decrements from 255 to 0 responsive to the clock signals, CLK and clock CLK 90.
>
> Manning, col. 5, lines 6-9.

Manning also teaches that inputs CLK and CLK 90 are "generated by a conventional clock circuit 28" (col. 4, lines 11-13).

In light of Manning's above teachings, it is Appellants' position that Manning's counter is not enabled and disabled *before/after receipt of each of a number of strobe signals*. Rather, it seems that Manning's counter 50 receives a pair of continuously generated clock signals, but only decrements (i.e., counts) in response to these clock signals during periods when it is enabled to do so. As a result, Manning's counter control logic differs from Appellants' counter control logic.

Appellants' claim 1 further recites that "counter control logic" resets a counter after each strobe signal is received by "receiving feedback from said counter". The Examiner asserts that such a reset based on counter "feedback" is taught by Manning in col. 5, lines 62-65. Appellants respectfully disagree.

As taught by Manning,

> . . .At or before the terminal count, other circuitry in the integrated circuit causes the STOP signal to go active high, thereby causing the Counter Control circuit 46 to disable the Counter 50.
>
> Manning, col. 5, lines 62-65.

Appellants believe it is too great a jump to conclude that the above statement supports the resetting of a counter based on feedback from the counter. Although Manning states that a STOP signal is caused to go active high "at or before the terminal count", Manning also states that it is "other circuitry in the integrated circuit" that causes the STOP signal to go active high (see also, Manning's col. 4, lines 64-67, wherein Manning states that the STOP signal is generated "elsewhere" by circuitry "not shown"). Manning does not state that the terminal count of the counter 50 is fed back to the "other circuitry". The Examiner only speculates that this is done. It is also possible that Manning's "other circuitry" merely asserts the STOP signal at a *predicted* time. In reality though, Manning says very little about how the "other circuitry" operates, and one can only speculate as to what Manning anticipated. Appellants believe the Examiner's particular speculation on how Manning's "other circuitry" works is based solely on hindsight reconstruction, using their own Specification as a guide. Such speculation is not sufficient to support a novelty rejection.

For the above reasons, Appellants' claim 1 is believed to be allowable over the teachings of Manning.

Appellants' claims 2-4 are believed to be allowable over Manning at least for the reason that they depend from claim 1.

Appellants' claim 5 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning. That is, Manning does not teach nor suggest "counter control logic" that 1) enables a counter "before *each* strobe signal is received", and 2) resets the counter "after *each* strobe signal is received".

Appellants' claims 6 and 9 are believed to be allowable over Manning at least

for the reason that they depend from claim 5.

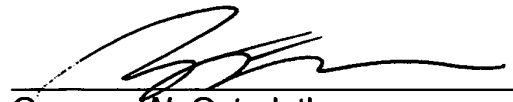
Appellants' claim 29 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning.

Appellants' claim 30 is believed to be allowable over Manning at least for the reason that it depends from claim 29.

Conclusion

In summary, the art of record does not teach nor suggest the subject matter of Appellants' claims 1-6, 9, 29 and 30. These claims are therefore believed to be allowable.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

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Appendix

Claim 1: Strobe receiver circuitry, comprising:

a) a counter, said counter updating a count in response to strobe edges of received strobe signals; and

b) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating control signals asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by receiving feedback from said counter and, in response to said feedback, resetting said counter asynchronously with respect to said received strobe signals.

Claim 2: Strobe receiver circuitry as in claim 1, wherein said control signal is a fixed width pulse.

Claim 3: Strobe receiver circuitry as in claim 1, wherein said control signal comprises start and stop conditions.

Claim 4: Strobe receiver circuitry as in claim 3, wherein said start and stop conditions are, respectively, falling and rising signal edges.

Claim 5: Strobe receiver circuitry, comprising:

a) a counter, said counter updating a count in response to strobe edges of received strobe signals; and

b) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions,

resetting said counter asynchronously with respect to said received strobe signals.

Claim 6: Strobe receiver circuitry as in claim 5, wherein each received strobe signal consists of a multiple of P strobe edges (P≥ 2), and wherein:

a) said counter is a rollover counter counting to P; and

b) said counter control logic generates said stop conditions during receipt of a last P strobe edges of each strobe signal.

Claim 7: Strobe receiver circuitry as in claim 6, wherein:

a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between when said counter control logic expects said counter to receive:

i) a first of a last P strobe edges of said late receipt case; and

ii) a last strobe edge of said early receipt case.

Claim 8: Strobe receiver circuitry as in claim 6, wherein:

a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between:

i) when said counter control logic expects said counter to receive a first of a last P strobe edges of said late receipt case; and

ii) an end of a postamble following said early receipt case.

Claim 9: Strobe receiver circuitry as in claim 5, wherein said start and stop conditions are generated on a single signal line.

Claim 10: Strobe receiver circuitry as in claim 5, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked by rising and falling edges of received strobe signals; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

Claim 11: Strobe receiver circuitry as in claim 10, wherein:

i) said first state element is a toggle flip-flop producing outputs SA and SA';

ii) said second state element is a toggle flip-flop producing outputs SB and SB';

iii) said first state element receives a reset input representing a logical AND of SA' and a single signal line on which said start and stop conditions are generated; and

iv) said second state element receives a reset input representing a logical AND of SA' and SB'.

Claim 12: Memory controller receiver circuitry, comprising:

a) a data pad and a strobe pad;

b) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being sequentially enabled to receive data by respective values of a count;

c) a counter, said counter updating said count in response to strobe edges of received strobe signals; and

d) counter control logic, said counter control logic enabling said counter

before each strobe signal is received by generating control signals asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by receiving feedback from said counter and, in response to said feedback, resetting said counter asynchronously with respect to said received strobe signals.

Claim 13: Memory controller receiver circuitry as in claim 12, wherein said control signal is a fixed width pulse.

Claim 14: Memory controller receiver circuitry as in claim 12, wherein said control signal comprises start and stop conditions.

Claim 15: Memory controller receiver circuitry as in claim 14, wherein said start and stop conditions are, respectively, falling and rising signal edges.

Claim 16: Memory controller receiver circuitry, comprising:

a) a data pad and a strobe pad;

b) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being sequentially enabled to receive data by respective values of a count;

c) a counter, said counter updating said count in response to strobe edges of strobe signals received at said strobe pad; and

d) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions, resetting said counter asynchronously with respect to said received strobe signals.

Claim 17: Memory controller receiver circuitry as in claim 16, wherein said counter control logic generates said stop condition at a time which is defined by whether a next read cycle will be:

a) a double data rate burst of four read cycle; or

b) a double data rate burst of eight read cycle.

Claim 18: Memory controller receiver circuitry as in claim 16, wherein said counter control logic generates said stop condition at a time which is defined by whether a next read cycle will be:

a) a 1x mode double data rate read cycle; or

b) an Mx mode double data rate read cycle ($M \geq 2$).

Claim 19: Memory controller receiver circuitry as in claim 16, wherein each received strobe signal consists of a multiple of P strobe edges, and wherein:

a) said counter is a rollover counter counting to P; and

b) said counter control logic generates said stop condition during receipt of a last P strobe edges of each strobe signal.

Claim 20: Memory controller receiver circuitry as in claim 19, wherein:

a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between when said counter control logic expects said counter to receive:

i) a first of a last P strobe edges of said late receipt case; and

ii) a last strobe edge of said early receipt case.

Claim 21: Memory controller receiver circuitry as in claim 19, wherein:

a) said counter control logic expects said counter to receive each strobe

signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between:

i) when said counter control logic expects said counter to receive a first of a last P strobe edges of said late receipt case; and

ii) an end of a postamble following said early receipt case.

Claim 22: Memory controller receiver circuitry as in claim 16, wherein said start and stop conditions are generated on a single signal line.

Claim 23: Memory controller receiver circuitry as in claim 16, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked by rising and falling edges of strobe signals received at said strobe pad; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

Claim 24: Memory controller receiver circuitry as in claim 23, wherein said rollover counter comprises P AND gates, each of which receives a different combination of outputs from said first and second state elements, and each of which produces one bit of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.

Claim 25: Memory controller receiver circuitry as in claim 23, wherein:

i) said first state element is a toggle flip-flop producing outputs SA and SA';

ii) said second state element is a toggle flip-flop producing outputs SB and SB';

iii) said first state element receives a reset input representing a logical AND of SA' and a single signal line on which said start and stop conditions are generated; and

iv) said second state element receives a reset input representing a logical AND of SA' and SB'.

Claim 26: Memory controller receiver circuitry as in claim 25, wherein said rollover counter comprises P AND gates which:

i) respectively receive flip-flop outputs SA' and SB', SA and SB', SA and SB, and SA' and SB; and

ii) respectively produce one bit each of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.

Claim 27: Memory controller receiver circuitry as in claim 16, wherein P=4.

Claim 28: A double data rate memory controller with tolerance for large variation in read loop delay, comprising:

a) data receiving means;

b) counting means for receiving and counting a number of strobe edges received during a memory read cycle;

c) means for controlling said data receiving means in response to a count produced by said counting means; and

d) means for enabling said counting means before each memory read cycle and resetting said counting means after each memory read cycle by i) enabling said counting means asynchronously with respect to said number of strobe edges, and ii) resetting said counting means asynchronously with respect to said number of strobe edges.

Claim 29: A method of receiving strobe signals into a memory controller, comprising:

a) enabling a strobe edge counter asynchronously with respect to said strobe signals, before each strobe signal is received, and in response to a start condition; and

b) resetting said strobe edge counter asynchronously with respect to said strobe signals, after each strobe signal is received, and in response to a combination of counter feedback and a stop condition.

Claim 30: A method as in claim 29, wherein each received strobe signal consists of a multiple of P strobe edges ($P \geq 2$), and wherein said counter is a rollover counter counting to P, the method further comprising:

generating said stop condition during receipt of a last P strobe edges of each strobe signal.

Claim 31: A method as in claim 30, wherein said counter receives each strobe signal at a time falling between an early receipt case and a late receipt case, the method further comprising:

generating said stop condition at a time falling between when said counter is expected to receive:

i) a first of a last P strobe edges of said late receipt case; and

ii) a last strobe edge of said early receipt case.

Claim 32: A method as in claim 30, wherein said counter receives each strobe signal at a time falling between an early receipt case and a late receipt case, the method further comprising:

generating said stop condition at a time falling between:

i) when said counter is expected to receive a first of a last P strobe edges of said late receipt case; and

ii) an end of a postamble following said early receipt case.

Claim 33: A method of receiving data into a memory controller, comprising, during a memory read cycle:

a) enabling a counter asynchronously with respect to a strobe signal, before the strobe signal is received at a strobe pad, and in response to a start condition;

b) storing sequential data bits received at a data pad in different ones of P storage elements ($P \geq 2$), in response to different values of a count produced by said counter; and

c) resetting said counter asynchronously with respect to said strobe signal, after the strobe signal is received, and in response to a combination of counter feedback and a stop condition.

Claim 34: A method as in claim 33, further comprising resetting said counter at different times, depending on whether a memory read cycle is:

a) a double data rate burst of four read cycle; or

b) a double data rate burst of eight read cycle.

Claim 35: A method as in claim 33, further comprising resetting said counter at different times, depending on whether a memory read cycle is:

a) a 1x mode double data rate read cycle; or

b) a 2x mode double data rate read cycle.

Claim 36: A computer system, comprising:

a) a CPU;

b) a memory controller coupled to said CPU;

c) an I/O controller coupled to said CPU;

d) a number of I/O devices coupled to said I/O controller; and

e) a number of memory modules coupled to said memory controller;

wherein said memory controller comprises a plurality of data and strobe pads to which are coupled receiver circuitry for receiving data and strobe signals from said memory modules; and

wherein said receiver circuitry comprises, for corresponding data and strobe pads:

i) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being sequentially enabled to receive data by respective values of a count;

ii) a counter, said counter updating said count in response to strobe edges of strobe signals received at said strobe pad; and

iii) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions, resetting said counter asynchronously with respect to said received strobe signals.

Claim 37: A computer system as in claim 36, wherein each of said P storage elements is a latch.

Claim 38: A computer system as in claim 36, wherein said count is a P-bit, one-high count, the bits of which respectively control ones of said P storage elements.

Claim 39: A computer system as in claim 36, wherein said memory controller and said I/O controller form an integrated memory and I/O controller.

Claim 40: A computer system as in claim 36, wherein said start and stop conditions are generated on a single signal line.

Claim 41: A computer system as in claim 36, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked by rising and falling edges of strobe signals received at said strobe pad; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

Claim 42: A computer system as in claim 41, wherein said rollover counter comprises P AND gates, each of which receives a different combination of outputs from said first and second state elements, and each of which produces one bit of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.